CCD Image Sensors and Analog-to-Digital Conversion

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Introduction

In today's world, many CCD imaging applications require digital processing. The first digital stage in any processing application involving CCDs will be converting the analog CCD signal[1] to the digital domain by employing an analog-to-digital converter. The design engineer is faced with several trade-offs including cost versus performance, speed of conversion versus bits of resolution, serial versus parallel conversion and finally, which CCD signal-processing techniques should be done in the analog domain and which in the digital domain.

The engineer should be aware of these trade-offs in order to optimize his particular design. This application note was written to consider these trade-offs in more detail and to consider the costs and benefits associated with each trade-off, thereby helping the engineer to optimize his design by making the correct choices. A typical application interface circuit is presented as well as the appropriate timing signals needed for a successful implementation of the circuit. Finally, a table of analog-to-digital converters and parameters relevant to these trade-offs is presented to assist the engineer in his selection.

Cost Versus Performance

In selecting an analog-to-digital converter for a particular CCD application, there is often a trade-off between cost and performance. Certain applications may require only low bit (i.e., coarse) resolution at very slow conversion rates. For example, the application may require only 4 bits of resolution at a 1-ms conversion rate[2] for very low cost. This can be easily accomplished with the Texas Instruments TL507 analog-to-digital converter. The cost versus performance trade-off is not an issue in this case. However, higher (i.e., finer) resolution and higher speed of conversion requirements may force a trade-off between one or the other of these requirements and cost. Therefore, it may not always be possible to maximize resolution and conversion speed while minimizing cost; the engineer will have to decide which are the most important requirements for the project.

Bit Resolution Versus Conversion Speed

Inherent in the analog-to-digital converter is the trade-off between bits of resolution and speed of conversion. This has special reference to digital conversion of the CCD output signal that typically has a dynamic range of 60 dB but can be increased to 73 dB with the use of correlated double sampling[3]. To digitally process the complete dynamic range of the sensor, the analog-to-digital converter must clearly have a dynamic range at least as great as the sensor's dynamic range. To convert dynamic range to bits, the units most often used to specify the resolution of an analog-to-digital converter, use the formula $N \geq (DR/6.02)$ with N being resolution and DR being dynamic range in dB. A CCD dynamic range of 60 dB requires an analog-to-digital converter of at least 10 bits while a CCD dynamic range of 73 dB requires an analog-to-digital converter of at least 13 bits. To convert the analog signal at a video rate (typically 7–20 MHz), a flash type analog-to-digital converter must be employed. This reduces the dynamic range of the system because a flash converter operating at a video-conversion rate typically has a resolution of 8 bits (48 dB)[4]. Conversely, if the complete dynamic range of the sensor is to be converted without loss of resolution, video rates of conversion cannot be achieved without significant impact on cost and power.

Serial Versus Parallel Conversion

Texas Instruments CCD output register formats include 1) one-register devices, 2) two- and three-register devices that can be shifted out in parallel, and 3) three register devices that require 120 degree phase differences between the three registers. If a CCD of format 1) is used, the serial versus parallel conversion trade-off does not arise as there is only one output channel. If a CCD of format 2) is used, the engineer faces the choice of analog multiplexing the multiple channels into one video stream that requires one analog-to-digital converter, or performing a digital conversion on each individual channel requiring multiple analog-to-digital converters, or finally, using an analog-to-digital converter with an on-board

multiplexer. The first solution requires an analog multiplexer[5] as well as multiplexer-select signals for control. This solution results in conversions that will not be maximized for speed as the channels are not converted in parallel. However, it saves the designer the cost and complexity of multiple analog-to-digital converters and a digital multiplexing operation once the data has been digitized. The second option is clearly the best for speed of conversion as the data can be converted in parallel. However, it will necessitate the additional cost and complexity of one or two more analog-to-digital converters and probably a digital multiplexer. Although the third choice is the slowest, it offers the lowest part count of the options. Only one analog-to-digital converter is required. In addition, external analog multiplexing is not required as the analog-to-digital converter has an on-board multiplexer. This solution requires generating input-channel select line signals. However, this may involve no more complexity than generating the signals for the analog multiplexer as in the first option. If a CCD of format 3) is used and fast conversion speed is desired, it makes no sense to use three analog-to-digital converters. There is no speed advantage in doing this, while at the same time tripling the part count. The two major conversion methods would then be using an analog multiplexer, one analog-to-digital converter, or a multiple channel analog-to-digital converter with an on-board multiplexer. The relative advantages and disadvantages of these have already been discussed. If speed is not important to the application, it may be cost effective to have three slow converters, one for each channel.

Analog Versus Digital Processing

In any digital processing application, the engineer must decide how much analog processing should be used before the digital conversion is made. Some analog-signal conditioning is usually required. Two necessary analog operations are dc restoring and amplification. DC restoring is necessary to set the black level of the CCD. This should be set to the minimum dc level input of the analog-to-digital converter that corresponds to the all-zero output in the digital domain. Amplification is necessary to gain the signal so that the CCD saturation level corresponds to the maximum dc input of the a-to-d. This corresponds to all-1s output in the digital domain. Additional CCD processing stages could be required such as sampling and holding[6], filtering, dark signal subtraction, gamma, and agc. With the exception of sampling and holding, which is an analog operation, these operations can be done in either the digital or in the analog domain. The engineer has to decide which processing operations should be analog and which should be digital according to his own unique application.

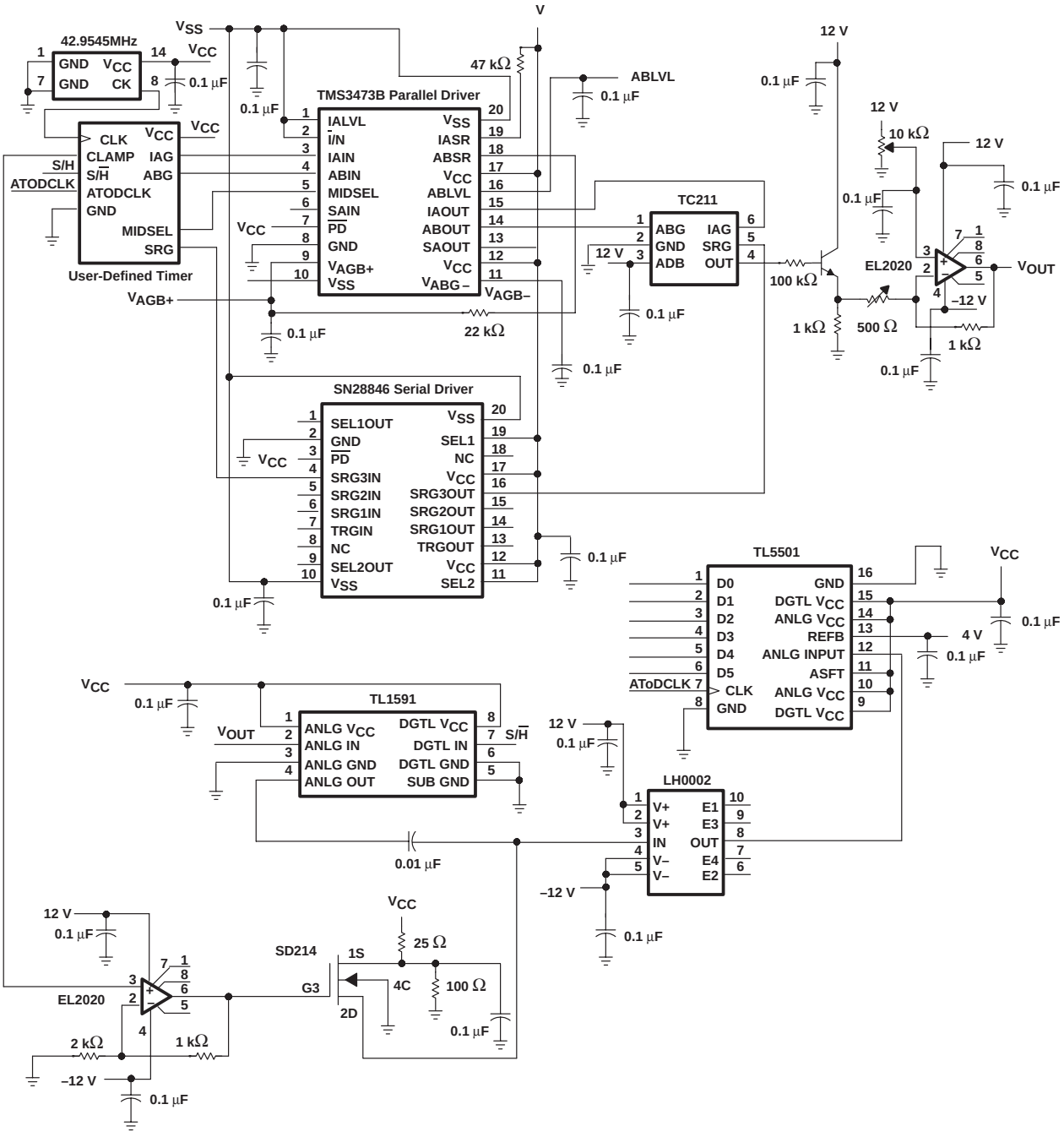
Typical CCD to A-to-D Interface Circuit

A typical CCD to analog-to-digital converter interface circuit is shown in Figure 1. The CCD is the Texas Instruments TC211 and the analog-to-digital converter is the Texas Instruments TL5501. A master oscillator clocks a user-defined timer which itself supplies all the CCD and video-processing signals for the rest of the circuit. The timer supplies TTL clock signals to the CCD drivers that level shift and slew rate adjust them for the CCD. The CCD signal is buffered by an emitter follower and amplified so that the full-well signal out of the sample-and-hold device is 1 V above the dark level. This ensures that the full-well signal corresponds to the maximum dc input voltage to the analog-to-digital converter. After sampling and holding, the signal is dc restored to 4 V, the minimum dc input voltage to the analog-to-digital converter. The signal is then buffered and fed to the TL5501 analog-to-digital converter. The timing signals needed for successful implementation of this circuit are shown in Figure 2. This circuit clearly illustrates one of the trade-offs discussed above. System-dynamic range is sacrificed in favor of a very high rate of conversion. The CCD has a dynamic range of 60 dB while the analog-to-digital converter has a bit resolution of only 6 bits (which corresponds to a dynamic range of 36 dB). However, the conversions are done at video rates.

Table 1 lists some of the more common Texas Instruments analog-to-digital converters along with parameters relevant to the engineering trade-offs previously discussed. Table 1 is by no means an exhaustive list.

Table 1. Analog-to-Digital Converter Parameters

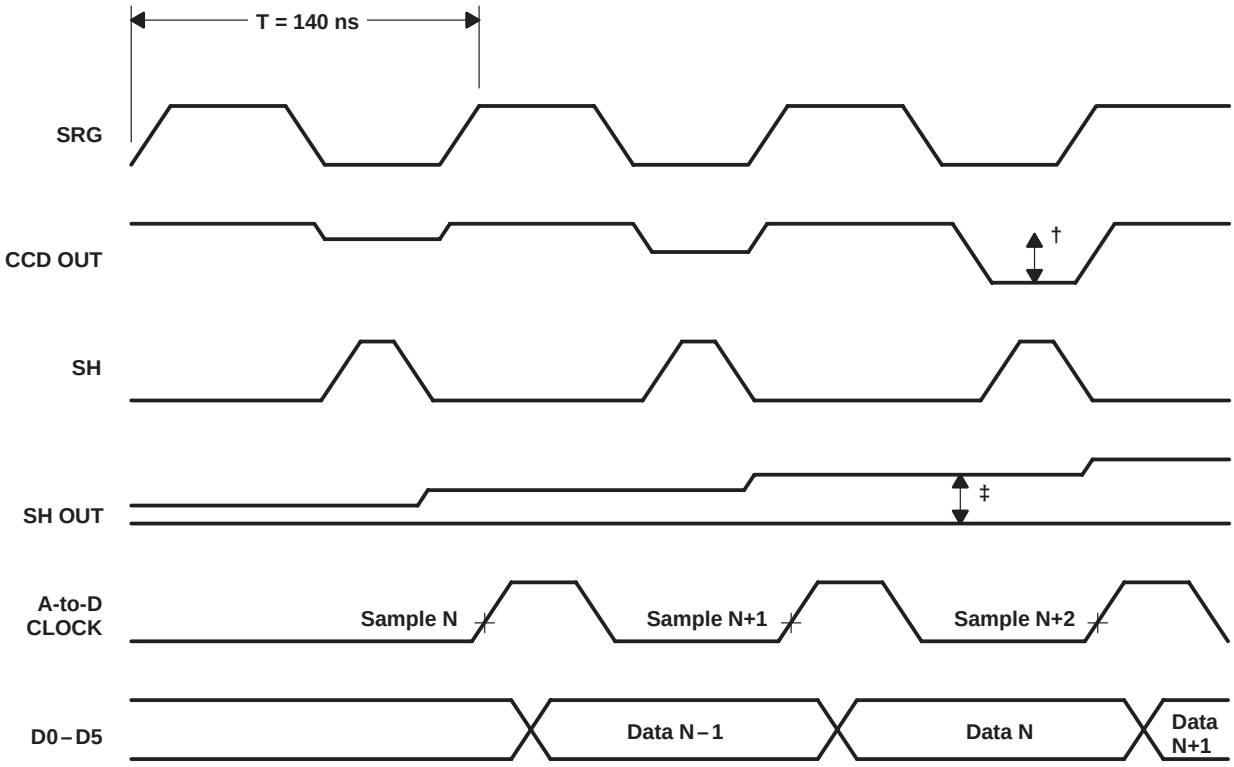
A-TO-D CONVERTER	RESOLUTION	CONVERSION SPEED	TYPE	UNIQUE FEATURES	BUDGETARY PRICE (2/93)
TL507	8 bits	1 ms	Ratiometric	Very low cost	1.11
ADC0808	8 bits	100 µs	Successive approximation	8-channel multiplexer	8.06
ADC0820	8 bits	1.18 µs	Modified flash		11.10
TL5501	6 bits	33 ns	Flash	Suitable for video rates	16.65
TL5503-2	8 bits	40 ns	Flash		16.65
TLC1225	12 bits	12 µs	Successive approximation	High dynamic range	17.76
TLC1550I	10 bits	6 µs	Successive approximation		9.99



DC VOLTAGES

V	2 V
V_{SS}	–10 V
V_{ABG+}	4 V
V_{ABG-}	–5 V
ABLVL	–2 V
V_{CC}	5 V

Figure 1. CCD to A-to-D Interface Circuit



† Magnitude is proportion to incoming light.
‡ Magnitude is proportional to CCD OUT.

Figure 2. CCD to A-to-D Timing Diagram

NOTES

1. Many people unfamiliar with CCD technology believe that the CCD is a digital device. Probably they are confusing it with a digital shift register. However, the CCD uses an analog shift register. The CCD output is an analog signal voltage directly proportional to incident light intensity.
2. At very slow conversion rates, it will probably be necessary to cool the device in order to prevent the build up of dark current.
3. There is an extensive literature on correlated double sampling (CDS) also known as correlated clamp sample and hold (CCSH) as a noise-reduction technique in CCDs. See, for example, "High-Resolution 8-mm CCD Image Sensor With Correlated Clamp Sample-and-Hold Charge Detection Circuit", IEEE Transactions on Electron Devices, Vol. ED-33, No. 6, June 1986, and "Theoretical Analysis and Optimization of CDS Signal Processing Method for CCD Image Sensors", IEEE Transactions on Electron Devices, Vol. 39, No. 11, November 1992, both by Dr. Jerry Hynecek.
4. Higher resolution flash converters of 10 and 12 bits do exist but they are extremely expensive. For example, the Analog Devices AD9020, which has a resolution of 10 bits and a conversion speed of 25 ns, resales for a cost greater than $200.00.
5. The analog multiplexer should, of course, be chosen so as not to degrade the dynamic range of the system.
6. Sampling and holding is critical with inherently slow converters such as successive-approximation converters. Otherwise, the successive approximations may be done on different output levels, leading to poor results.